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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/091,698	03/05/2002	Brian N. Ripley	100202181-1	7441

7590 11/06/2003

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EXAMINER	
INOA, MIDYS	

ART UNIT	PAPER NUMBER
2188	5

DATE MAILED: 11/06/2003

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/091,698	BRIAN RIPLEY	
	Examiner	Art Unit	
	Midys Inoa	2188	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *21 May 2002* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-25* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-19,21,22,24 and 25* is/are rejected.

7)☒ Claim(s) *20 and 23* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *05 March 2002* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449) Paper No(s) _____ .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other:

DETAILED ACTION

Drawings

1. The drawings filed on March 5th, 2002 have been accepted by the examiner.

Claim Rejections - 35 USC § 112

2. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

3. Claims 1-7 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding Claim 1, when read in context, it is not understood what is meant by the phrase "said plurality of memory locations store information and bit width of at least two of said memory locations **are different**". It is unclear what limitations are being identified as different.

Claims 2-7 are rejected as having the same deficiencies as the Claim they depend from.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-18, 21 are rejected under 35 U.S.C. 102(e) as being anticipated by Triece et al. (US 2003/0005254 A1).

Regarding Claims 1, 4-5, 21-22, 24, Triece teaches a system in which a memory is addressed based on variable word width ("variable width memory"). In this system, the memory communicates with other processor components through a bus 150; this bus thus allows communication with each address in the memory ("memory locations", Page 5, paragraph 0059). It is understood that each memory location is uniquely identified by each unique memory address. Triece's system discloses basing the variable word width as a multiple of a byte width (Page 1, paragraph 0007). In addition, the system teaches a series of control devices such as instruction units and program counters (Figure 1) which directly interface with the memory and thus control access to it as well as monitor communications between components.

Regarding Claim 2, since a memory comprises of memory addresses, it is understood that each of these memory addresses are in the same substrate as the memory.

Regarding Claim 3, it is understood that the memory of Triece's system could be a RAM.

Regarding Claim 6, since byte widths determined the word width of the memory, it is understood that if two words have the same width in the memory, then the byte widths should be the same.

Regarding Claim 7, it is understood that addressing a memory with variable word widths usually has the effect of reducing processor operations.

Regarding Claims 8-15, Triece teaches a system in which a memory is addressed based on variable word width ("variable width memory"). This is done through use of a processor fetching function and decoding such instruction based in byte/word bits and upper/lower bits ("register indicators", "data block configuration"). The control signals generated then determines if the memory will be accessed. In this system, the memory

communicates with other processor components through a bus 150; this bus thus allows communication with each address in the memory ("memory locations", Page 5, paragraphs 0059-0062). It is understood that each memory location is uniquely identified by each unique memory address. In accessing the memory, the memory is transferring information to the processor, which has the same byte width determining the variable word width. It is understood that an access to the memory can be a store or a read. It is understood that addressing a memory with variable word widths usually has the effect of reducing processor operations

Regarding Claims 16-18, as in all memories, the variable width memory of Triece et al. has many memory locations uniquely identified by memory addresses, which could be known as external identifiers.

Regarding Claim 25, Triece et al. teaches the use of a processor fetching function and a decoder to determine of a memory will be accessed using byte/word bits and upper/lower bits ("register indicators", "data block configuration", Page 5, paragraphs 0059-0061).

Claim Rejections - 35 USC § 103

6. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

7. Claim 19 is rejected under 35 U.S.C. 103(a) as being unpatentable over Triece et al. (US 2003/0005254 A1). Triece et al. does not teach arranging width bits in a contiguous manner. It would have been obvious to one of ordinary skill in the art at the time the invention was made to arrange the width bits in a contiguous manner for easier access.

Allowable Subject Matter

8. Claims 20 and 23 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Regarding Claim 20, the Prior Art of Record does not teach arranging data blocks according to a communications packet configuration.

Regarding Claim 23, the Prior Art of Record does not teach storing means that returns a number of bits equal to the width of one unique memory location.

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Midys Inoa whose telephone number is (703) 305-7850. The examiner can normally be reached on M-F 7:00am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (703) 306-2903. The fax phone number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Midys Inoa
Examiner
Art Unit 2188

MI

11/3/03

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER
TC 21